An Innovative Method for Direct Wideband Measurement of ADC Aperture Jitter and SNR

Adam C. Escobar
SEAKR Engineering, Inc.
6221 S Racine Circle
Centennial, CO 80111
adam.escobar@seakr.com
ph: 720-446-2630

Abstract

Under-sampling an analog signal is now a common practice in analog-to-digital conversion. At high sampling frequencies, the ADC aperture jitter dominates the noise environment. The ADC aperture jitter and any additive jitter in the path to the sampling clock input affects the available signal-to-noise ratio with greater degradation for under-sampling applications. This paper explains a new non-invasive time domain test method to determine the jitter with sub-picosecond resolution.

Introduction

The use of today's high sampling rate low noise ADCs allows for the ability for higher input frequencies. From Kester (2015), the Shannon-Nyquist theorem permits an analog signal with a defined bandwidth to be sampled in a region of input frequencies bounded between

$$\frac{(n-1)f_s}{2} < f_{in} < \frac{nf_s}{2}, \qquad \textbf{Eq- 1}$$

where f_s is the sampling rate; f_{in} is the analog input frequency, and n is the Nyquist zone. In order to not lose information, the entire bandwidth of the input signal has to be contained within one of these regions. This paper concentrates on the 3rd Nyquist zone (n = 3); however, the jitter measurement method explained here is applicable for oversampling conditions as well.

As explained later in the paper, at high frequencies (f_{in} > 100 MHz), the available ADC signal-to-noise-ratio (SNR) is primarily dependent on the total system jitter, especially for under-sampling. Specific under-sampling applications include direct RF recording, direct IF recording (also called Pre-D recording), and frequency hopping. Numerous engineers have developed and improved test methods to determine the jitter by: 1) total SNR measurement method, 2) phase noise integration method, or 3) dual input zero-crossing method. This paper provides a time domain method that improves upon existing methods, allowing for: direct jitter measurement, wideband jitter performance, system SNR analysis, and less data collection and processing in order to obtain sub-picosecond resolution of ADC aperture jitter. In order to verify this, then this paper provides simulation and measurement results.

ADC Signal-to-Noise Ratio Overview

Prior to presenting the SNR jitter measurement method, the paper provides a SNR derivation overview for an ADC. SNR depends upon the noise environment of the particular system. The predominant noise contributors for an ADC application are: quantization noise, thermal noise, sampling clock jitter, ADC aperture jitter, and the analog input jitter (phase noise). From Ostemeir (2010), the quantization noise degrades the SNR, such that the maximum theoretical SNR for a given ADC bit resolution is

$$\mathrm{SNR}_q = 20\log\left(2^{No.\ bits}\sqrt{\frac{3}{2}}\right). \qquad \textbf{Eq- 2}$$

Therefore, as expected for a particular ADC resolution, the SNR cannot be better than this value. If over-sampling (Nyquist region #1), then the SNR improves to

$$\mathrm{SNR}_q = 20\log\left(2^{No.\ bits-1}\sqrt{3}\sqrt{\frac{f_s}{f_{in}}}\right). \qquad \textbf{Eq- 3}$$

The thermal noise is usually taken into account by the composite RMS differential non-linearity (DNL) measurement of an ADC. This measurement is taken at a low frequency (f_{in} < 10 MHz), where thermal noise dominates. The thermal noise effect on SNR is found with

$$\mathrm{SNR}_{th} = -20\log\left(\frac{1+\mathrm{DNL}}{2^{No.\ bits}}\right). \qquad \textbf{Eq- 4}$$

The three jitter terms can be consolidated to form a total jitter, t_j,

$$t_j = \sqrt{t_{j\_CLK}^2 + t_{j\_ADC}^2 + t_{j\_IN}^2}\,, \qquad \textbf{Eq- 5}$$

where t_{j_CLK} is the clock jitter; t_{j_ADC} is the ADC aperture jitter, and t_{j_IN} is the analog input jitter. The effect that total jitter has on the SNR is

$$\mathrm{SNR}_j = 20\log\left(\frac{1}{2\pi f_{in} t_j}\right). \qquad \textbf{Eq- 6}$$

With the above SNR contributions listed, the total SNR dependency can be represented by the following relationship:

$$\mathrm{SNR}[\mathrm{dB}] = -10\log\left(10^{\frac{\mathrm{SNR}_q}{10}} + 10^{\frac{\mathrm{SNR}_{th}}{10}} + 10^{\frac{\mathrm{SNR}_j}{10}}\right)$$

Eq- 7

Fig-1 provides a typical relationship of a 12-bit ADC's SNR as a function of frequency. The plot lists the typical noise parameters used. As explained previously, the total jitter dominates the effect on the SNR at high frequencies. The sampling clock frequency was chosen such that the frequency range of interest was in the third Nyquist zone, which for sampling IF and RF frequencies, this frequency range is usually in the jitter dominated region.

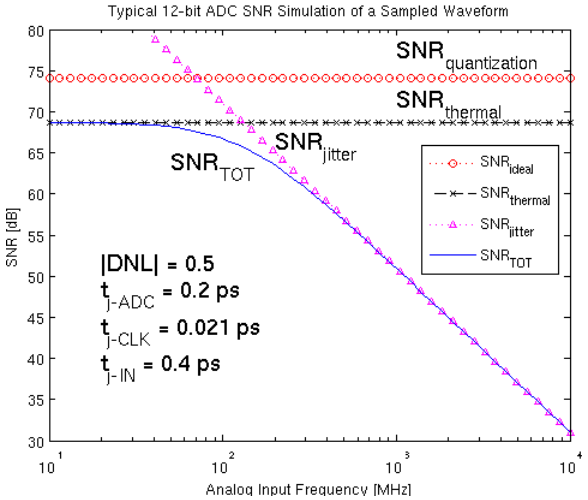

Fig-1. Simulation of the SNR for a state-of-the art 12-bit ADC under test with the effect of the signal generator. This simulation highlights the jitter dominated region at high sampling frequencies.

Review: SNR Jitter Measurement Method

The SNR jitter measurement method includes acquiring the phase noise density plot of the sampled signal and then backing out the jitter portion from all the noise sources. The stimulus is usually a continuous wave (CW) signal of known frequency. The SNR derivation is accomplished by a discrete Fourier transform, specifically the Fast Fourier Transform (FFT). SNR measurements can also be obtained through other signal processing means, which is explained later. The SNR is calculated from integrating the entire noise power throughout the bandwidth of the system. This SNR derivation does not account for the close-in noise. Fig-2 depicts the two regions that contribute to the total noise. The close-in noise is located adjacent to the input carrier frequency, and the broadband proceeds up until the bandwidth of the system. There are two issues with taking the FFT: 1) the input waveform that is being sampled has to be at the center of a frequency bin in order to mitigate spectral leakage and 2) the close-in noise may be difficult to measure because the number of samples used to generate the FFT limits the frequency resolution. For example, a sample size of 32768 samples generates frequency steps of 18.311 kHz; therefore, the close-in phase noise from 10 Hz to 18.311 kHz from carrier would just be attributed to signal power. In order to obtain close-in noise information, then a larger sample set is required following the relationship for the frequency bin size, f_{bin}:

$$f_{bin} = \frac{f_s}{No.\ \ of\ \ Samples}\,. \qquad \textbf{Eq- 8}$$

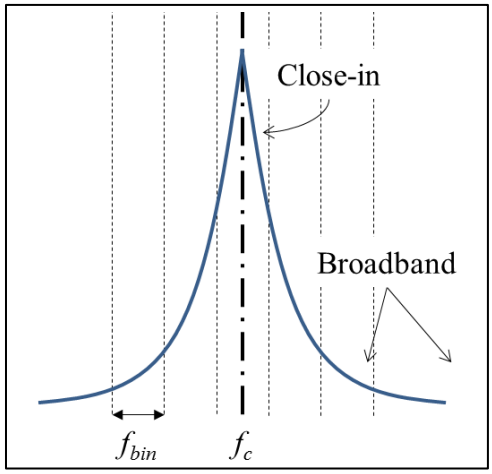

Fig-2. Representation of close-in and broadband phase noise. Note the close-in noise is located completely within the f_{bin} of the CW signal.

There also exists a relationship to determine the particular input frequency in order for the CW input to be at the center of a frequency bin. If the previous equation was multiplied with an odd natural number, *x*, such that the multiplier to the sample rate was mutually prime, then the result provides an input frequency at the center of a frequency bin:

$$f_{in} = f_s \cdot \frac{x}{No.\ of\ \ Samples} \qquad \textbf{Eq- 9}$$

Once the SNR is found by using the FFT, then the total jitter can be calculated through subtracting the other sources of noise using Eq- 2 to Eq- 7.

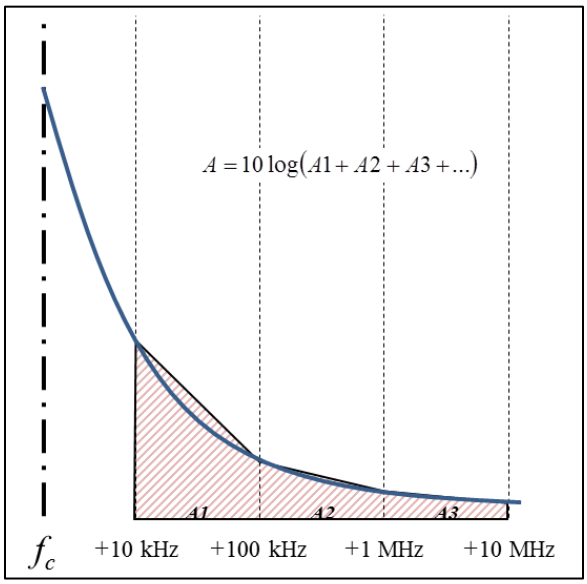

Fig-3. Example plot depicting phase noise density approximation to calculate phase jitter.

Review: Phase Noise Integration Method

The phase noise integration method is a second method to determine the jitter directly. Since this paper concentrates on the jitter dominated region, Kester (2009) provided a method to calculate the total RMS jitter from a phase noise density spectrum by integrating the area under the phase noise density plot; however, the close-in phase noise is still not taken into account:

$$t_j = \frac{\sqrt{2 \cdot 10^{A/10}}}{2\pi f_c}, \qquad \textbf{Eq- 10}$$

where *A* is the area under the curve (noise power, P_n). This method is similar to the SNR jitter measurement method by utilizing an FFT. The close-in noise is still omitted and is contributed to the signal power. Fig-3 shows an approximation for the integration under the phase noise spectrum.

Review: Dual Input Zero-Crossing Method

The dual input zero-crossing method is a time domain method that is a direct measurement to determine the total jitter. Lundberg (2002) has shown that jitter is associated with the RMS voltage error due to the shift in time (jitter) of taking the input waveform sample. Fig-4 illustrates the possible variance of sample retrieval due to the effect of jitter. The maximum change in voltage occurs at the zero-crossings of a continuous wave (CW) signal. Since the input waveform is a CW signal, the input voltage is

$$V_{in} = V_A \sin(\omega_{in} t + \phi), \qquad \textbf{Eq- 11}$$

where V_A is the amplitude of the input signal. The maximum slope is then

$$\frac{d}{dt} V_{in}\Big|_{\max} = 2\pi f_{in} V_A; \qquad \textbf{Eq- 12}$$

therefore, the RMS jitter is the denominator of the left side. Solving provides

$$t_j = \frac{V_{err}}{2\pi f_{in} V_A}, \qquad \textbf{Eq- 13}$$

where V_{err} is the RMS Voltage error of the zero-crossing samples.

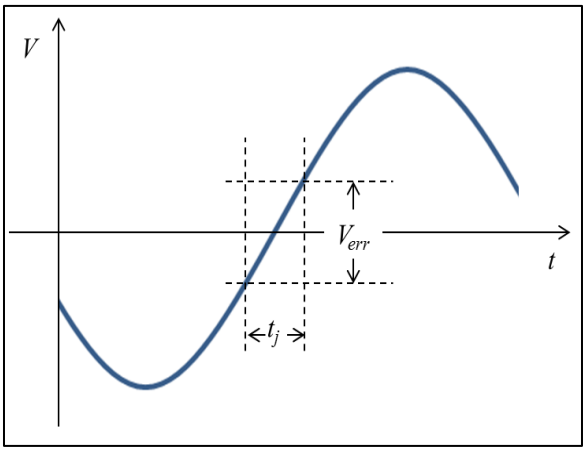

Fig-4. Plot illustrating the RMS voltage error related to the RMS jitter.

Lundberg developed the idea to send a single CW signal of the same frequency to both the analog input and the sampling clock input. This allows the sampled waveform to only be a constant value. In order to obtain the zero-crossing samples, the phase of the analog input and sampling clock input must differ by either 0° or 180°. Once the phase was set properly, then the RMS voltage value can be found. Total jitter is solved using Eq- 13.

A key issue with this method is that the data only exists at one frequency point for the ADC. If the ADC under test has a set sampling rate, because the application requires a certain region of interest, then it may not be feasible to either apply the sampling clock frequency, f_s, at the analog input, f_{in}, or alter the sampling clock frequency. There may be filters, baluns, or other circuit elements that do not allow certain frequencies to be applied at either input. The concept of sampling zero-crossings is the basis for the new measurement method that is explained in the next section.

Wideband Zero-Crossing Method

The wideband zero-crossing method is the newly developed method to determine ADC aperture jitter with sub-picosecond resolution and system SNR. The theory stems from the dual input zero-crossing method, where the RMS error voltage at the zero-crossing is used to determine the total jitter. The CW stimulus at the analog input is the same as the previous method; however, the sampling clock is at a fixed frequency. This allows for determining jitter in any Nyquist region. The wideband zero-crossing method involves: 1) determining multiple frequencies across the specific Nyquist region of interest that contains zero-crossing samples, 2) phase aligning the input analog signal to the input clock, and 3) processing the extracted zero-crossing samples.

1) Determining Acceptable Frequencies

The first step is to determine the applicable frequencies in a particular Nyquist region that contain periodic zero crossing samples. As stated previously, this method of determining aperture jitter can be applied to both over-sampling and under-sampling cases; therefore, from Eq- 1, the frequencies in Nyquist zones, n, (n = 1, 2, 3, …) can be used to determine jitter for any particular application. Determined during the investigation, the periodic nature of the zero-crossing input frequencies, f_{in}, relating to the sampling clock, f_s, followed the pattern below:

$$f_{in}(i) = \begin{cases} \frac{f_s}{2}\left(n + \frac{1}{i} - 1\right) & ; \quad \frac{(n-1)f_s}{2} < f \le f_{mid} \\ \frac{f_s}{2}\left(n - \frac{1}{i}\right) & ; \quad f_{mid} < f < \frac{nf_s}{2} \end{cases}$$

Eq- 14,

where i is the number of time steps between zero-crossing samples (i = 2,3,4,…), and f_{mid} is the frequency marking the middle of a particular Nyquist region, which is equal to

$$f_{mid} = \left(\frac{(2n-1)f_s}{4}\right). \qquad \textbf{Eq- 15}$$

Eq- 14 provides a set of input frequencies, f_{in}, that include periodic zero-crossing samples for a particular sampling clock frequency, f_s, and Nyquist region, n. This set of input frequencies still has one issue, which is phase alignment with the sampling time of the ADC under test.

Realistically, RF cables, test equipment, and PCB routing are not phase matched. Even though the input frequency follows the zero-crossing equation, the sampling instance of the ADC may not be aligned with the zero-crossing of the input signal. The next section explains a simple method to phase align the input to the sampling clock of the ADC.

2) Phase Alignment

The second step involves aligning the phase of the input. The available sine wave generators today include phase-locked signal generation based on a reference oscillator, which can be either an internal or external reference. By using the same reference oscillator for the generation of the analog input signal and the sampling clock, the two signals to the ADC can be phased aligned. Shifting the input signal for any phase offset aligns the two signals at the ADC. Fig-7 provides an interface diagram of the entire system under test. Typical phase resolutions for low end equipment are 0.1 degree steps, which is more than sufficient as will be seen in simulation.

In under-sampling applications, phase matching utilizes the lower aliased frequency. The phase offset associated with the aliased signal, so happens to equal a change in phase in the actual applied higher frequency signal. There are a few different methods to measure the phase offset between two signals: 1) Fast Fourier Transform, 2) Single Frequency DFT, 3) Trigonometric Identities, 4) Cross-Correlation, and 5) Hilbert Transform. The FFT cannot be used in this application, because

the frequency under test may not align to the center of a frequency bin. The single frequency DFT is the easiest method. Using trigonometric properties requires a measurement of amplitude, which is accomplished by one of the other processing methods. Lastly, the cross correlation is dependent on the sampling rate. Either the single frequency DFT or Hilbert transform can be used reliably.

Prior to taking the first measurement, the ADC system requires the full-scale range (FSR) to be calibrated. As seen in Eq- 13, the jitter measurement is dependent on the measured amplitude. In order to determine the phase offset of the input signal, a test sample set is recorded. The sampled data is analyzed for the amplitude, V_A, of the input CW signal. This test sample set is then compared to an ideal waveform, $s(t)_{ideal}$, with a phase of zero. Using the amplitude just calculated from the sample set,

$$s(t)_{ideal} = V_A \sin(2\pi f_{in} t). \qquad \textbf{Eq- 16}$$

The cross-correlation or the Hilbert transform is then used to determine the phase difference of the input signal to the ideal zero phase signal. The signal generator for the analog input is then programmed with this phase difference. The result is a phased matched signal to the ideal signal with zero phase difference. The resulting wave may start at a sample that is not the zero-crossing sample, but these samples can be simply removed in post-processing until a zero-crossing sample is found. Fig-5 provides an example of a simulation for phase shifting a random phase signal to the ideal phase to provide zero-crossing samples.

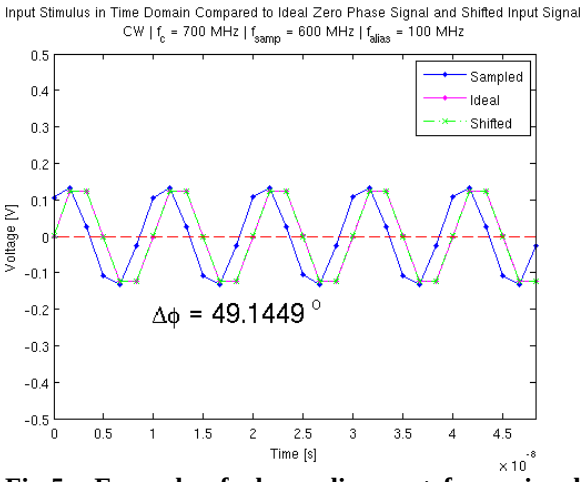

Fig-5. Example of phase alignment for a signal sampled in the 3rd Nyquist zone (f_{in} = 700 MHz, f_s = 600 MHz).

3) Processing Data for Total Jitter

In processing the newly sampled phase adjusted signal, the zero-crossing samples need to be extracted into an array. To extract the zero-crossing samples, the first zero-crossing sample needs to be found in a dataset. Once this sample is found, then all the zero-crossing samples can be extracted according to Eq- 14. Due to the resolution of the phase alignment, there may be a DC value associated with the positive slope samples and one with the negative slope samples. This DC value has to be subtracted, such that the mean value is found for each set and removed. After this is accomplished, then Eq- 13 can be used to find the total jitter by calculating the RMS value for the dataset. After the signal generator and sampling clock are calibrated for jitter, Eq- 5 provides the aperture jitter. The next section reviews simulations of this method.

Total Jitter Simulation

This section investigates the acceptable range of measurement error for the phase and amplitude that corresponds to the effect on the total jitter of the sampled waveform. A simulation for the system under test was accomplished for varying phase and amplitude offsets from ideal. Table 1 provides the simulation parameters, except for the simulation injected RMS jitter, which was 0.5 ps. The simulation results have also been integrated over 100 iterations.

In order to obtain a properly represented input signal, the injected jitter for the stimulus contains a normalized (Gaussian) distribution of jitter from the RMS value (standard deviation). The time jitter, t_j, is represented as

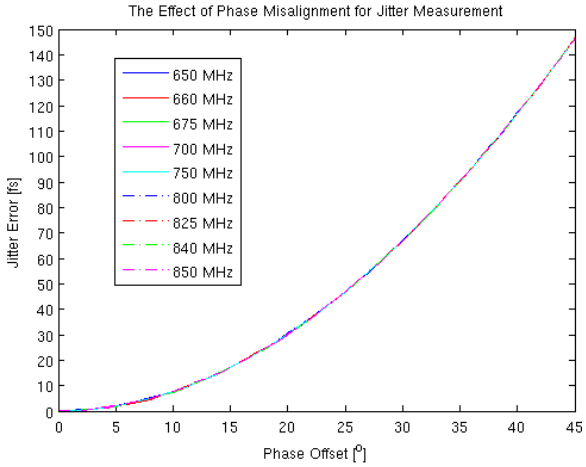

Fig-6. Simulation displaying phase offset's effect on jitter error. Notice that the effect of phase offset is frequency independent.

$$t_j = \mu + \sigma \cdot P(t), \qquad \textbf{Eq- 17}$$

where μ is the mean jitter value; σ is the standard deviation (RMS), and $P(t)$ is the probability density function, which is that of a normalized distribution. The mean, μ, is zero for this simulation, because the jitter is set around the ideal case of zero jitter. With this set of jitter values, the input stimulus is

$$s(t) = \Delta V_A \sin\left(2\pi f_{in}\left(t + t_j\right) + \Delta\phi\right) \qquad \textbf{Eq- 18}$$

where $\Delta\phi$ is the phase offset and ΔV_A is the amplitude offset. The amplitude was held constant at -5.0 dBm during the phase offset simulation, and the phase offset was held constant at 0° during the amplitude offset simulation.

Fig-6 and Fig-7 represent the simulation results for the phase offset and amplitude offset iterations, respectively. As seen in the plots, the effect of phase and amplitude offsets relative to the jitter error is frequency independent. With 100 iterations, the average error in the ideal case was found to be ~1.2 fs, and with 1000 iterations it was found to be ~0.2 fs; therefore, integration of larger sample sets decreases error.

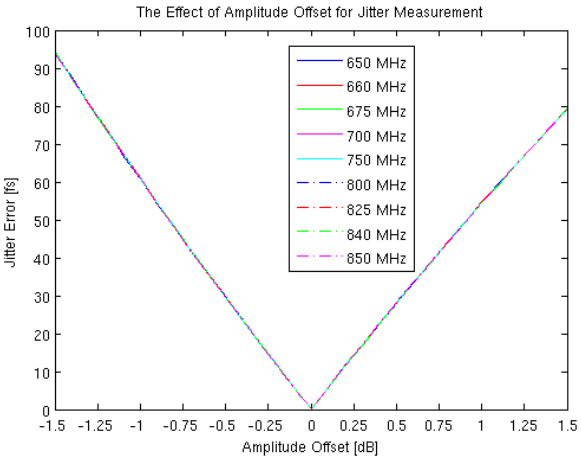

Fig-7. Simulation displaying amplitude offset's effect on jitter error. Notice that the effect of amplitude offset is frequency independent.

Looking closer at the phase offset simulation, a good figure of merit is to keep the phase offset less than ~8°. This allows for jitter errors on the magnitude of ~5 fs. This is easily accomplished with the low-end signal generators available in the market. For the second simulation, the amplitude offset has a larger effect on the jitter error. For ~5 fs error under the amplitude offset simulation, then the amplitude requires a measurement to an accuracy of ~0.1 dB. This is achievable with utilizing the Hilbert transform and conducting a calibration of the FSR for the ADC.

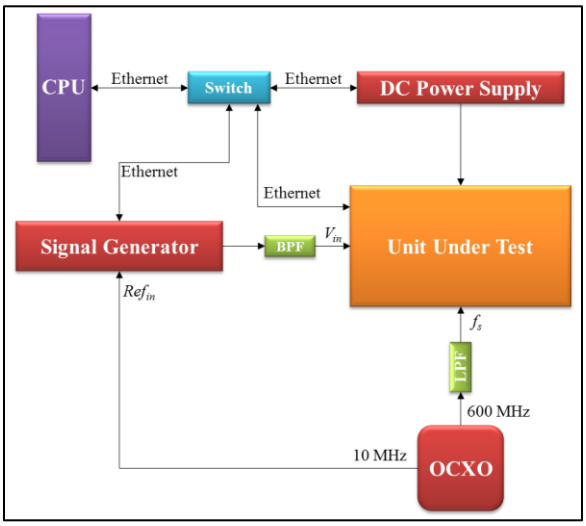

Fig-8. Interface diagram for system under test and test system.

System Under Test and Test System

As previously stated, the system operated in the 3rd Nyquist region. Table 1 lists the test parameters for this region. Since the sampling clock is 600 MHz, the region of interest for ADC input frequencies is 600–900 MHz; however, only a 200 MHz bandwidth was required for the application, so the tested region was 650–850 MHz. Fig-8 provides an interface diagram of the entire system. The entire system was controlled via Ethernet using a primary control computer.

Table 1 - Test Parameters to Measure Total Jitter

Test Parameter	Value	Unit
Min. Input Frequency	650	MHz
Max. Input Frequency	850	MHz
Sampling Clock	600	MHz
FSR	+5.0	dBm
Stimulus RF Power	-5.0	dBm
Number of Samples	32768	-
Number of Iterations	10	-

The system under test contains a state-of-the-art high sample rate ADC. SEAKR developed the hardware and FPGA design for interfacing to this ADC. The ADC was configured for use in a low power mode for use in the 3rd Nyquist region. Table

2 provides common specifications of the ADC for this region.

Table 2 - Typical 12-bit ADC Specifications

Parameter	Typical Value	Unit
Resolution	12	bits
Power Consumption	2.5	W
ENOB	9.3	bits
SNR	58.2	dBFSR
SFDR	67.3	dBFSR
|DNL|	0.5	LSB

The test system utilized commercial-off-the-shelf (COTS) equipment. A signal generator created the analog input stimulus, V_{in}. An oven controlled oscillator (OCXO) provided the 10 MHz and 600 MHz, f_s, reference clocks. Using an OCXO minimizes the phase noise and its effect on total jitter measurements. The 10 MHz reference provided the external reference for the signal generator. A 220 MHz band-pass filter was used for the signal generator output, and a 615 MHz low-pass filter was used for the sampling clock output.

Measurement Results and Discussion

This section presents the measurement and analysis of the total jitter and SNR. Fig-9 displays the measured total jitter and the measured aperture jitter. Eq- 13 and Eq- 14 provided the solution for the measured total jitter as analyzed from sampled zero-crossing data points. The theoretical total jitter was calculated from the measured signal generator jitter, measured sample clock jitter, and theoretical ADC aperture jitter. The measured total jitter matches the theoretical closely. Notice that the total jitter is decreasing with an increase of frequency. At first glance, it may be counterintuitive to have this relationship, except the total jitter follows the trend of the dominant source of jitter, the signal generator jitter.

The measured ADC aperture jitter contains the aperture jitter of the ADC, as well as the additive jitter for all the components in-line with the sampling clock signal to the ADC. This is the reason for the slightly higher value of aperture jitter versus the ADC typical value. This is also the reason for the slightly higher total jitter above the theoretical simulation.

The total jitter and aperture jitter provide the SNR of the system by using Eq- 6. Fig-10 depicts the resulting SNR from the jitter measurements. The total jitter is dominated by the signal generator phase noise, and this can be seen in the SNR relationship. If just the measured aperture jitter were used for SNR calculation, then the result provides the actual noise environment of the system; this is called the system SNR. The system SNR is the optimal output SNR possible regardless of the input SNR. The system SNR can be improved by designing low additive jitter components for the sampling clock input.

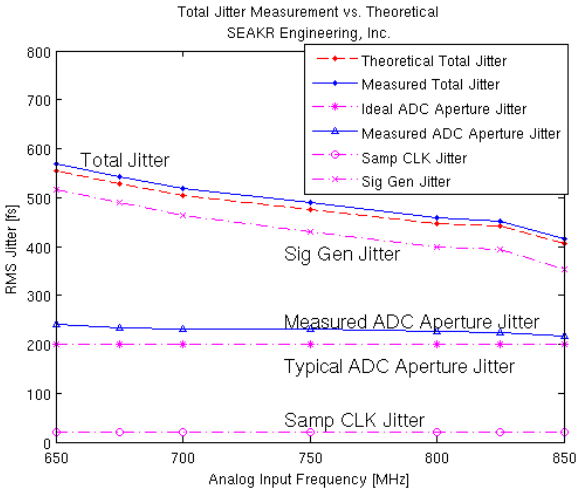

Fig-9. Measurement results for total jitter and ADC aperture jitter. The signal generator is the dominant source of the total jitter. The measured ADC aperture jitter includes additive jitter for all components between the OCXO output and the ADC sampling clock input.

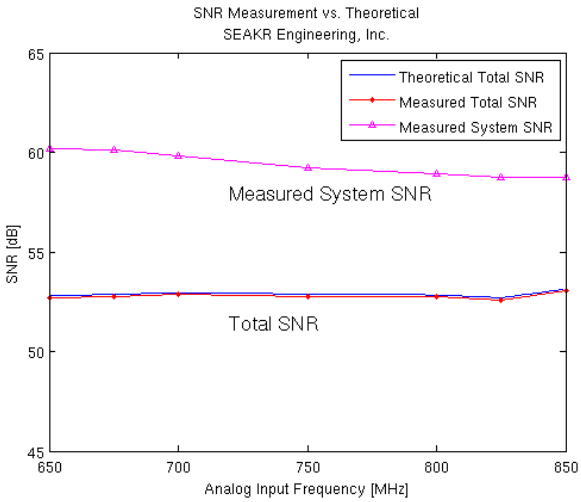

Fig - 10. The plot illustrates the total SNR and the system SNR. The total SNR is a result of the total jitter, including: signal generator, sampling clock, and ADC aperture jitter. The system SNR is strictly a result of the measured aperture jitter.

Conclusions

The paper demonstrated a new technique to directly measure ADC aperture jitter and SNR by way of the wideband zero-crossing method. This method is capable of measurements in any Nyquist region for over-sampling and under-sampling applications. This is a wideband method, where the frequencies of interest have been chosen according to Eq- 14 for a certain Nyquist region. This equation provides for the zero-crossing samples at certain intervals. Once these zero-crossing samples have been extracted and processed, Eq- 13 and Eq- 5 are used for total jitter and aperture jitter calculation, and SNR is found by Eq- 6. It has also been shown that careful design implementations, as well as test equipment selection is necessary for obtaining sub-picosecond jitter measurements.

For high resolution of the aperture jitter and system SNR, then large sample sets are needed. Through simulation, it was found that 100 iterations of sample sets of size 32768 samples provided resolutions in the range of a few femto-seconds. Depending on the application then a single iteration or smaller sample sets may be sufficient.

The key requirements for the test equipment include: a coherent time reference between the analog input signal and the sampling clock input, phase noise (jitter) calibration of both sources, and a band-limited system. The coherency of the reference oscillator is necessary in order to incorporate the phase adjustments at the signal generator. The phase jitter calibration for the signal generator and the sampling clock are necessary to accurately determine the aperture jitter, which is found by subtracting the squared jitter of the external sources from the squared total jitter and taking the square root.

The measured aperture jitter includes all the additive jitter from the output of the sampling clock to the ADC sampling input circuitry. The aperture jitter can increase if the ADC sampling clock phase adjust is used; therefore, it is critical to make all calibrations and adjustments after any aperture delays are set. To minimize the aperture jitter, then the clock interface components need to be chosen carefully, and the aperture delay setting should be as small as possible (if used). If the sampling clock is part of the system under test, then an oscillator with low phase noise should be chosen.

For using the wideband zero-crossing method to measure system SNR, the system SNR that was calculated in this paper was located in a region for noise dominated by jitter of the particular ADC (usually high frequencies > 100 MHz). If lower frequencies are of interest, then the thermal noise will have to be taken into account. Thermal noise can be measured at lower frequencies (~10 MHz or less), where this noise is the dominant noise for an ADC. Using Eq- 7 and following the zero-crossing method still provides aperture jitter and system SNR measurements. For example, the range telemetry community usually utilizes a 2nd IF of 70 MHz output from their receivers. This can be directly sampled using an ADC for pre-D recording. If the ADC that is mentioned in this paper is used, then as seen in Fig-1, the total SNR has contributing factors from both thermal and jitter noise sources. The system SNR would have to take both sources into account.

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